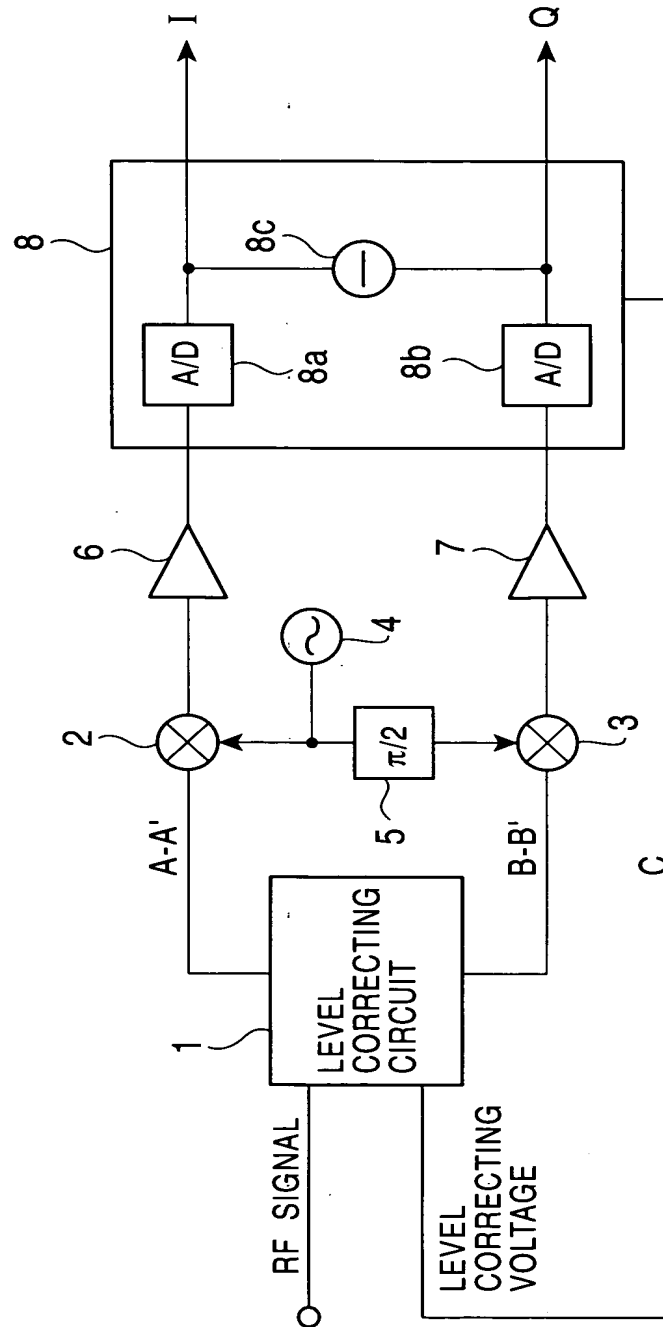


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FIG. 1



The diagram illustrates a level correction circuit. It starts with an RF signal input at the bottom left, which passes through a series of transistors (11, 12, 14, 15, 18, 19) and resistors (16, 17, 20, 21) connected in a ladder-like structure. A level correcting voltage is applied to the gates of transistors 14, 15, 18, and 19. The output is taken from a node between resistors 16 and 17, labeled A. Other nodes are labeled B, A', and B'. A ground symbol is shown at the bottom.

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FIG. 3
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